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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,048	06/25/2004	Arild Wego	P16145-US1	9119

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EXAMINER	
RUTKOWSKI, JEFFREY M	
ART UNIT	PAPER NUMBER
2619	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/500,048	WEGO ET AL.	
	Examiner	Art Unit	
	Jeffrey M. Rutkowski	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-10 have been cancelled.

Information Disclosure Statement

1. The information disclosure statement filed 06/25/2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered. This objection is raised again because no copies of the prior art have been made of record.

Specification

2. The disclosure is objected to because of the following informalities: there appears to be some typographical errors on pages 8 and 12 of the specification. On page 8 lines 19-21 it appears the numbers 22,625 and 0,625 are errors. The specification seems to suggest the comma should be replaced by a decimal point, making the number 22.625 and 0.625 respectively. The same error occurs on page 12 lines 25-28. Appropriate correction is required.

Claim Objections

3. **Claim 12** is objected to because of the following informalities: it appears the word bite on the second line of the claim should be changed to byte. Appropriate correction is required.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. **Claim 11** is provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over **claim 10** of copending Application No. 10/526526, hereinafter referred to as the '526 application, in view of Acharya (US Pat 7,110,359). **Claim 11** of the present application is essentially the same as **claim 10** of the '526 application. The timer recited in **claim 11** of the present application and the counter recited in **claim 10** of the '526 application are essentially the same since both are being used for buffer management functions and a timer is another type of counter.

6. **Claim 10** of the '526 application does not recite the use of a scheduler. Acharya makes up for the scheduler deficiency by disclosing the use of a scheduler in a multi-port switch **[figure 2]**. It would have been obvious to a person of ordinary skill in the art at

the time of the invention to use a scheduler in the '526 application to control access to memory.

This is a provisional obviousness-type double patenting rejection.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. **Claims 15 and 20** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what the constant value of 131.072 MHz represents. For example, the constant value could represent a master system clock frequency or the clocking frequency of an interface (interface rate).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

11. **Claims 11-12, 14, 17-19** are rejected under 35 U.S.C. 103(a) as being unpatentable over McHarg et al. (US Pat 5,291,482), hereinafter referred to as McHarg in view of Acharya (US Pat 7,110,359).

12. For **claims 11 and 17**, McHarg teaches a high bandwidth packet switch **[title]**. The switch contains a time multiplexed write **210** and read **212** bus **[col. 5 lines 25-30 and figure 2]** (one or more time slot buses for transferring frames from a number of serial input/output lines located on a receiving side of the node to a number of serial output lines located. on the transmitting side of the node). A buffer is connected between the input and output ports. A buffer manager uses pointers to allocate memory locations for storing packets **[abstract]** (one or two data buffers for each time slot bus at the receiving side of the node for buffering the frames from the input/output lines before transmission, said one or two data buffers being shared between all the input/output lines by means of respective pointers allocating one memory area in a data buffer for each of the input/output lines). A monitor circuit uses a timer to determine if a pointer is encountered within a certain time period **[col. 15 lines 30-33]** (a timer for each input/output line for indicating the time at which data transfer requests for the respective input/output line are to occur). Packet receivers **202** and transmitters **204** are connected to the time multiplexed write **210** and read **212** buses. McHarg does not teach the First In First Out (FIFO) buffers for each serial line or the use of a scheduler. Acharya teaches the FIFO limitation absent from the teachings of McHarg by disclosing a multiport switch

with a receiver and a transmitter which include a respective FIFO buffer **[col. 3 lines 60-63 and col. 7 lines 5-10]** (the serial input/output lines each having one respective FIFO into/from which bits corresponding to the associated serial line are shifted). Acharya teaches the scheduler limitation absent from the teachings of McHarg by disclosing the use of a scheduler **220 [figure 2]**.

13. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use FIFO buffers for each serial line in McHarg's invention to protect a level of burst protection. It also would have been obvious to a person of ordinary skill in the art at the time of the invention to use a scheduler in McHarg's invention to control access to memory.

14. For **claim 12 and 18**, the combination of McHarg and Acharya teach everything in **claims 11 and 17**. The teachings of McHarg in the rejection of **claims 11 and 17** discuss the pointer being used for storing memory location information (wherein a pointer contains a data bus address of the first bite of the data area it is allocating).

15. For **claims 14 and 19**, the combination of McHarg and Acharya teach everything in parent **claims 11 and 17**. McHarg does not teach the use of a round-robin scheduling mechanism. Acharya teaches the round-robin scheduling limitation absent from the teachings of McHarg by disclosing a network device that uses weighted round-robin scheduling to service queues **[abstract]** (wherein the scheduler checks the input lines for data transfer requests by using a round-robin scheme on a transfer request register containing one entry for each input line indicating if a data transfer request for the respective input lines exists).

16. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a weighted round-robin scheduling mechanism in McHarg's invention to cure an overflow condition.

17. **Claim 13** is rejected under 35 U.S.C. 103(a) as being unpatentable over McHarg as modified by Acharya as applied to **claim 11** above, and further in view of Reid (US Pat 4,131,762).

18. For **claim 13**, the combination of McHarg and Acharya teach everything in parent **claim 11**. McHarg teaches a lookup table used by a router **208** maps logical destination to a physical packet channel number, which is then used to select a transmitter pointer FIFO **[col. 6 lines 22-27]** (wherein there is one connection table for each time slot bus at the receiving side, each entry in the connection table contains at least a data bus address pointing to a byte in the associated data buffer, the entries are arranged in the same order as their corresponding bytes are to be transferred on the data bus). McHarg does not teach the use of a time-slot counter. Reid teaches the time-slot counter limitation absent from the teachings of McHarg by disclosing a time-slot counter is synchronized to a precision clock **[col. 7 lines 27-30 and figure 12]** (a counter, synchronized to a clock used by the time slot bus for transmission of timeslots, indicates which byte in the associated data buffer that presently is to be read out from the data bus buffer into a time slot in the associated data bus by indexing the entries of the connection table).

19. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a time-slot counter in McHarg's invention to generate memory addresses **[Reid, col. 7 lines 15-20]**.

20. **Claim 16** is rejected under 35 U.S.C. 103(a) as being unpatentable over McHarg as modified by Acharya applied to **claim 11** above, and further in view of Sanders et al. (US Pat 6,931,022), hereinafter referred to as Sanders.

21. For **claim 16**, the combination of McHarg and Acharya teach everything in parent **claim 11**. McHarg does not teach a minimum delay modus or a constant delay modus. Sanders teaches the dual operating modus absent from the teachings of McHarg by disclosing a time slot interchanger operates in a minimum delay mode or a constant delay mode **[col. 4 lines 38-44]** (wherein frames are transmitted through the time slot buses either in a minimum delay modus or in a constant delay modus; in case of minimum delay, bytes from an input line are transferred over a time slot bus in the same order as they arrived on the input line; and, in the case of constant delay, bytes in transfer on a time slot bus are identifiable and bytes from an input line may be transferred over a time slot bus in an order different from the order they arrived on the input line).

22. It would have been obvious to a person of ordinary skill in the art at the time of the invention to use a dual operating modus (minimum delay or constant delay) in McHarg's invention to allow support for more than one transmission technique.

Response to Arguments

23. Arguments:

McHarg's buffer is a centralized component. In the claimed invention, the TDM bus is a centralized component.

McHarg teaches that a pointer is distributed to the packet receiver where it is used to calculate an address that is sent over the write-bus to the buffer where the address is used as a write address for incoming data. The claimed invention does not operate in this manner.

McHarg teaches that a timer is used for determining whether a pointer is encountered within a certain time period. This has no relation to the function of the timer recited in the Applicant's independent claims 11 and 17.

Response:

There is no structural difference between McHarg's invention and the claimed invention. Since Mc Harg's invention is capable of performing the intended use, Mc Harg's invention meets the limitations of the claims.

24. Argument:

McHarg relates to a packet switch, while the claimed invention relates to a time division multiplexed (TDM)-based switch.

Response:

The applicant claims a "communications network node" containing some of the same structural elements found in the teachings of Mc Harg. A

"communications network node" could either be a packet switch or a TDM switch.

25. Argument:

The combination of McHarg and Acharya is technically improper because the combination is not operable. In a packet switch as disclosed by McHarg, the packets are transferred to the buffer immediately upon arrival. Therefore, the addition of the scheduler from Acharya is meaningless and would not be considered by one of ordinary skill in the art.

Response:

Mc Harg teaches the router queues packets upon arrival **[col. 2 lines 55-68]**. A person of ordinary skill in the art would be driven to Acharya's scheduler to find a way to manage Mc Harg's queues.

26. Applicant's arguments filed 12/10/2007 have been fully considered but they are not persuasive, for the reasons stated above.

Allowable Subject Matter

27. **Claims 15 and 20** would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey M. Rutkowski whose telephone number is (571)

270-1215. The examiner can normally be reached on Monday - Friday 7:30-5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jeffrey M Rutkowski
Patent Examiner
12/28/2007

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